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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/836,375	04/17/2001	Peter W. Cook	YOR9-2000-0402US1 (8728-4	5195

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EXAMINER
SURYAWANSHI, SURESH

ART UNIT	PAPER NUMBER
2115	5

DATE MAILED: 04/02/2004

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Please find below and/or attached an Office communication concerning this application or proceeding.

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Office Action Summary	Application No.	Applicant(s)	
	09/836,375	COOK ET AL.	
	Examiner	Art Unit	
	Suresh K Suryawanshi	2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE ____ MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 April 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 June 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-15 are presented for examination.

Drawings

2. Figures 1A, 1B, 2A and 2B should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

3. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4) because reference character "306" has been used to designate "Logic I", "Logic j" and "Logic k". A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

4. The disclosure is objected to because of the following informalities: symbol "18" should have been "18" at page 3, line 13.

Appropriate correction is required.

5. The disclosure is objected to because of the following informalities: symbol "506" is not found in the figure 9A as mentioned at page 18, line 18.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

7. Claims 1-15 are rejected under 35 U.S.C. 102(a) as being anticipated by Schuster et al (Asynchronous Interlocked Pipelined CMOS Circuits Operating at 3.3-4.5GHz; ISSCC 2000/February 9, 2000[1]).

8. As per claim 1, Schuster et al teach

a first logic circuit [Figure 17.3.2; Logic];

a latch coupled to a second logic circuit of an adjacent stage [Figure 17.3.2; Latch];

[1] Reference cited by applicants in paper no 4.

a switch which connects the first logic circuit to the latch in a first stage and disconnects the logic circuit from the latch in a second stage [Figure 17.3.3a; Switch circuit];

a local clock circuit which controls the first and second states by providing a locally generated clock signal to activate the switch, the locally generated clock signals being generated by interlocking handshake signals from a local clock circuit of an adjacent stage [Figure 17.3.2; Local Clock circuit; Handshaking; page 292; paragraph 4; locally generated clocks for each stage are active only when the data to a given stage is valid].

9. As per claim 9, Schuster et al teach

providing, for each stage, a latch connected to an input of that stage and a switch for selectively coupling the input of the stage to an output of the previous stage [Figure 17.3.2; Latch; Figure 17.3.3a; Switch];

when the data is valid in a current stage, sending a valid signal to a local clock circuit of a next stage of the plurality of stages [Figure 17.3.2; Figure 17.3.2; VALID signal; page 292; paragraph 4; locally generated clocks for each stage are active only when the data to a given stage is valid];

sending an acknowledge signal from the local clock circuit of the next stage to a local clock circuit of the current stage responsive to the valid signal [Figure 17.3.2; ACK signal; page 292; paragraph 6];

generating a local clock signal at the local clock circuit of the current stage of the plurality of stages based on the acknowledge signal and the valid signal [Figure 17.3.2; Local Clock circuit generating local clock signal based on the acknowledge (ACK) signal]; and

enabling the switch of the current stage based on the local clock signal to permit data transfer to the latch of the current stage from the output of the previous stage [Figure 17.3.2; Figure 17.3.3a; page 292; paragraph 4-6].

10. As per claim 2, Schuster et al teach that the interlocking handshake signal include an acknowledge signal from a downstream local clock circuit [Figure 17.3.2; ACK signal] and a valid signal from an upstream local clock circuit [Figure 17.3.2; VALID signal].

11. As per claim 3, Schuster et al teach that the local clock circuit outputs the locally generated clock responsive to the acknowledge signal and the valid signal [Figure 17.3.2; Local Clock circuit generating local clock signal based on the acknowledge (ACK) signal].

12. As per claim 4, Schuster et al teach that the interlocking handshake signal guarantee that when a current latch is enabled a latch of a previous stage and a latch of subsequent stage are disabled [Figure 17.3.2; page 292; paragraph 6].

13. As per claim 5, Schuster et al teach that local clock circuit for each stage is enabled only when there is an operation to perform [page 292, paragraph 4].

14. As per claim 6, Schuster et al teach that each stage includes a scan chain which permits data to be input and output to each stage in accordance with an external clock [page 292; paragraph 6; external valid signal].

15. As per claims 7 and 14, Schuster et al teach that the latch includes a first end connected to the switch and a second end connected to a data scan latch, the data latch scan latch connecting the second end of the latch to a first end of a next corresponding latch of an adjacent stage such that data is scanned into or out of the latch through the data scan latch [Figure 17.3.2; Figure 17.3.3a; page 292; paragraphs 4-6].

16. As per claim 8, Schuster et al teach that the circuit includes an asynchronous pipeline [Figure 17.3.2; Asynchronous Handshaking].

17. As per claim 10, Schuster et al teach the step of interlocking the local clock circuits [Figure 17.3.2; page 292; paragraph 6].

18. As per claim 11, Schuster et al teach the step of disabling the switch of the current stage during operation of an adjacent stage [Figure 17.3.2; Figure 17.3.3a; page 292; paragraph 4-6].

19. As per claim 12, Schuster et al teach the step of generating a local clock signal at the local clock circuit of the current stage include enabling the local clock circuit for each stage only when there is an operation to perform [Figure 17.3.2; Local Clock circuit generating local clock signal based on the acknowledge (ACK) signal; page 292, paragraph 4-6].

20. As per claim 13, Schuster et al teach that each stage includes a scan chain which permits a data to be input and output to each stage in accordance with an external clock [page 292; paragraph 6; external valid signal].

21. As per claim 15, Schuster et al teach the step of selectively enabling the switches to perform data scanning [Figure 17.3.2; Figure 17.3.3a; page 292; paragraph 4-6].

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Suresh K Suryawanshi whose telephone number is 703-305-3990. The examiner can normally be reached on 9:00am - 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas C. Lee can be reached on 703-305-9717. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

sks
March 29, 2004

THOMAS LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100